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EXAMINER
AUDUONG, GENE NGHIA

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/002,607	Applicant(s) BERGEMONT ET AL.	
	Examiner Gene N Auduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 May 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on May 2, 2002. These drawings are acceptable.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 1, 2002 is being considered by the examiner.

Claim Objections

3. Claim 3 is objected to because of the following informalities: Claim 3, line 1, the limitation "The array of claim 3" seems to be written as --The array of claim 2--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Randolph et al. (U.S.Pat. No. 5,949,718).

Regarding claim 1, Randolph et al. disclose an array of flash type nonvolatile memory cells arranged in a plurality of rows and columns (see figure 2) comprising: a wordline associated with each row of the array (word lines 108, 118, 128 and 138); a bitline associated with each column of the array (bit lines 142, 144, 146, 148, 150 and 152); a plurality of flash

type nonvolatile memory transistors (flash type, non-volatile memory cells 102-107, 112-117, 122-127 and 132-137), each of the flash type nonvolatile memory transistors associated with one row and one column in the array, each flash type nonvolatile memory transistor having a source, a drain, a floating gate and a control gate, the control gate of each flash type nonvolatile memory transistor coupled to the one of the wordlines with which its row is associated (the control gate of flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137 coupled to one of the word lines 108, 118, 128 and 138), the drain of each flash type nonvolatile memory transistor coupled to the one of the bitlines with which its column is associated (the drain of flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137 coupled to one of the bit lines 142, 144, 146, 148, 150 and 152); the source of each flash type nonvolatile memory transistor in a row of the array coupled together (source of memory transistor 102-107 in a row coupled together by a source lines 110); and a source transistor associated with each row of the array (source select transistors 101, 111, 121 and 131), each source transistor having a gate coupled to the one of the wordlines with which its row is associated (gate of source transistors 101, 111, 121 and 131 coupled to the word lines 108, 118, 128 and 138), a source coupled to a source potential line (source of select transistors 101, 111, 121 and 131 are coupled to ground potential), and a drain coupled to the sources of each flash type nonvolatile memory transistor with which its row is associated (drain of source transistor 101 connected to the source of memory transistors 102-107 by the source line 110; figure 2, col. 4, lines 45-64).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Randolph et al. (U.S. Pat. No. 5,949,718) in view of Lee et al. (U.S. Pat. No. 6,243,298).

Regarding claim 4, Randolph et al. disclose an array of nonvolatile memory cells arranged in a plurality of rows and columns (see figure 2) comprising: a wordline associated with each row of the array (word lines 108, 118, 128 and 138); a bitline associated with each column of the array (bit lines 142, 144, 146, 148, 150 and 152); a plurality of flash memory transistors (flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137), each of the flash type non-volatile memory transistor associated with one row and one column in the array, each flash type non-volatile memory transistor having a source, a drain, a floating gate and a control gate, the control gate of each flash nonvolatile memory transistor coupled to the one of the wordlines with which its row is associated (the control gate of the flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137 coupled to one of the word lines 108, 118, 128 and 138), the drain of each flash type nonvolatile memory transistor coupled to the one of the bitlines with which its column is associated (the drain of flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137 coupled to one of the bit lines 142, 144, 146, 148, 150 and 152); the source of each flash type nonvolatile memory transistor in adjacent pairs of rows of the array coupled together (see figure 2, source of memory transistors 102 and 112 coupled together to the source line 110); and a source transistor associated with each row of the array (source select transistors 101, 111, 121 and 131) each the source transistor having a gate coupled to the one of the wordlines with which its row is associated (gate of source

transistors 101, 111, 121 and 131 coupled to the word lines 108, 118, 128 and 138), a source coupled to a source potential line (source of select transistors 101, 111, 121 and 131 coupled to the ground potential), and a drain coupled to the sources of each nonvolatile memory transistor with which its row is associated (a drain of the source transistor 101 coupled to the source of memory transistors 102-107 by the source line 110; figure 2, col. 4, lines 45-64). Randolph et al. do not explicitly disclose the flash type non-volatile memory is a split-gate non-volatile memory.

Lee et al. disclose a flash memory cell as in figures 1, 6 and 7 capable of being programmed and erased through substantially separate areas of one of its drain-side and source side region comprising the teaching: there are various type of non-volatile semiconductor memory devices. These including ROM (Read-Only-Memory), the memory cell is permanently programmed, EPROM (Erasable Programmable Read-Only-Memory), EEPROM (Electrically Erasable Programmable Read-Only-Memory), and flash memory is another type of non-volatile memory. Several different types of flash memory cell structures have been developed, including split-gate type, triple poly erase cell, etc., they have been known and used by one skill in the art (see Lee et al., col. 1, lines 22-45). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type as design choice.

Regarding claim 5, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 4. Randolph et al. do not specifically disclose the array of cell disposing in an isolation well.

However, Lee et al. further disclose each of the memory cells include source and drain are space apart in p-type silicon substrate (p-type well) is met as claimed the array of cell disposing in an isolation well (forming in silicon substrate; col. 5, lines 26-41). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice.

Regarding claim 6, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 5. Randolph et al. do not specifically disclose the array of claim 5 further comprising a well selection transistor coupled to the isolation well.

However, Lee et al. further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage (subthreshold) leakage (see figure 2, 3 and 5). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice, and further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage leakage.

Regarding claim 7, Randolph et al. disclose an array of nonvolatile memory cells arranged in a plurality of rows and columns (see figure 2) comprising: a wordline (word lines

108, 118, 128 and 138) associated with each row of the array; a bitline (bit-lines 142, 144, 146, 148 and 150) associated with each column of the array; a plurality of nonvolatile memory transistors (flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137), each of the nonvolatile memory transistors associated with one row and one column in the array, each nonvolatile memory transistor having a source, a drain, and a floating gate, the source of each nonvolatile memory transistor coupled to the one of the wordlines with which its row is associated (the source of memory transistor 102-107 in a row coupled together by a source lines 110), the drain of each nonvolatile memory transistor coupled to the one of the bitlines with which its column is associated (the drain of flash type, non-volatile memory transistors 102-107, 112-117, 122-127 and 132-137 coupled to one of the bit lines 142, 144, 146, 148, 150 and 152); and a source transistor associated with each row of the array (source of select transistors 101, 111, 121 and 131) each the source transistor having a gate coupled to the one of the wordlines with which its row is associated (gate of source transistors 101, 111, 121 and 131 coupled to the word lines 108, 118, 128 and 138), a source coupled to a source potential line (source of select transistors 101, 111, 121 and 131 coupled to the ground potential), and a drain coupled to the sources of each nonvolatile memory transistor with which its row is associated (a drain of the source transistor 101 coupled to the source of memory transistors 102-107 by the source line 110; figure 2, col. 4, lines 45-64). Randolph et al. do not explicitly disclose the non-volatile memory is a one-time programmable non-volatile memory as stated in the preamble of the claim.

Lee et al. disclose a flash memory cell as in figures 1, 6 and 7 capable of being programmed and erased through substantially separate areas of one of its drain-side and source side region comprising the teaching: there are various type of non-volatile semiconductor

memory devices. These including ROM (Read-Only-Memory), the memory cell is permanently programmed, EPROM (Erasable Programmable Read-Only-Memory), EEPROM (Electrically Erasable Programmable Read-Only-Memory), and flash memory is another type of non-volatile memory. Several different types of flash memory cell structures have been developed, including split-gate type, triple poly erase cell, etc., they have been known and used by one skill in the art (see Lee et al., col. 1, lines 22-45). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using a one-time programmable non-volatile memory as stated in the preamble of the claim or using any other known memory transistor type as design choice.

Regarding claim 8, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 7. Randolph et al. do not specifically disclose the array of cell disposing in an isolation well.

However, Lee et al. further disclose each of the memory cells include source and drain are space apart in p-type silicon substrate (p-type well) is met as claimed the array of cell disposing in an isolation well (forming in silicon substrate; col. 5, lines 26-41). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice.

Regarding claim 9, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 8. Randolph et al. do not specifically disclose the array of claim 8 further comprising a well selection transistor coupled to the isolation well.

However, Lee et al. further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage (subthreshold) leakage (see figure 2, 3 and 5). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice, and further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage leakage.

Regarding claim 2, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 1. Randolph et al. do not specifically disclose the array of cell disposing in an isolation well.

However, Lee et al. further disclose each of the memory cells include source and drain are space apart in p-type silicon substrate (p-type well) is met as claimed the array of cell disposing in an isolation well (forming in silicon substrate; col. 5, lines 26-41). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice.

Regarding claim 3, as best understood, Randolph et al. in view of Lee et al. disclosed all of the limitation as previously discussed in claim 2. Randolph et al. do not specifically disclose the array of claim 2 further comprising a well selection transistor coupled to the isolation well.

However, Lee et al. further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage (subthreshold) leakage (see figure 2, 3 and 5). Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to include Lee's teaching into Randolph's system to further claiming the system is using split-gate type non-volatile memory transistor or using any other known memory transistor type, and the memory array is disposing in an isolation well (forming in the silicon substrate) as design choice, and further disclose the substrate of the memory cell array is coupled and powered by the substrate potential, which is enabled or disabled by a switch or selection transistor for reducing the substrate voltage leakage.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shimada (U.S. Pat. No. 6,272,046),

Park et al. (U.S. Pat. No. 6,288,938).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
November 1, 2002

Gene N Auduong
Examiner
Art Unit 2818